WHAT IS CLAIMED IS:

1. A method of manufacturing a semiconductor device, the method comprising:

forming a lateral double-diffused metal oxide semiconductor (LDMOS) device in a substrate, the LDMOS device including a drain;

forming a first guard ring around and proximate the drain of the LDMOS device; and

forming a second guard ring around the first guard ring.

2. The method according to Claim 1, wherein forming the first guard ring and forming the second guard ring comprise forming a ring from a semiconductive material.

3. The method according to Claim 1, wherein forming the first guard ring comprises forming a P+ base guard ring, and wherein forming the second guard ring comprises forming an N+ collector guard ring.

4. The method according to Claim 3, wherein the first guard ring and the second guard ring form a parasitic transistor, wherein the parasitic transistor electrically isolates the drain of the LDMOS.

5. The method according to Claim 1, wherein forming the LDMOS device comprises providing a substrate, forming an N+ buried layer in a top portion of the substrate, and depositing a P-epitaxial layer over the N+ buried layer.

6. The method according to Claim 5, wherein depositing the P-epitaxial layer comprises depositing about 9-10 μm of doped semiconductor material.

7. The method according to Claim 5, further comprising forming a deep N-well in the P-epitaxial layer, wherein forming the first or second guard ring comprises forming the first or second guard ring in the deep N-well.

8. The method according to Claim 7, wherein forming the deep N-well comprises forming the deep N-well in the entire thickness of the P-epitaxial layer.

9. A method of manufacturing a lateral double-diffused metal oxide semiconductor (LDMOS) device, the method comprising:

providing a substrate, the substrate comprising a first semiconductor type;

forming a first pad dielectric on a top surface of the substrate;

forming a buried layer in a top region of the substrate, the buried layer comprising a second semiconductor type;

removing the first pad dielectric;

depositing a doped semiconductor material over the buried layer, the doped semiconductor material being doped with the first semiconductor type;

forming a second pad dielectric over the doped semiconductor material;

doping a portion of the doped semiconductor material to form a deep well region, the deep well region comprising an annular ring shape;

doping a portion of the doped semiconductor material to form at least one first high voltage well region;

doping a portion of the doped semiconductor material to form a second high voltage well region, the second high voltage well region comprising an annular shape disposed within a central portion of the annular deep well region;

depositing a dielectric layer over the second pad dielectric;

patterning the dielectric layer;

removing exposed portions of the second pad dielectric;

forming field dielectric over portions of the second high voltage well region and the at least one first high voltage well region using the dielectric layer as a mask;

removing the dielectric layer and remaining portions of the second pad dielectric;

forming a gate dielectric and gate of the LDMOS device over portions of the second high voltage well region, the at least one first high voltage well region, and a portion of the field dielectric;

simultaneously doping the annular deep well region, a portion of the second high voltage well region and a portion of the at least one first high voltage well region with a dopant of the second semiconductor type to form a first guard ring in the deep well region, a source of the LDMOS device in the second high voltage well region, and a drain of the LDMOS device in the at least one first high voltage well region; and

doping a portion of the annular second high voltage well region with a dopant of the first semiconductor type to form a second guard ring in the second high voltage well region, the second guard ring being formed in a central region of the first guard ring.

10. The method according to Claim 9, wherein the first semiconductor type comprises P-type, wherein the second semiconductor type comprises N+, wherein the deep well region comprises an N-well, wherein the at least one first high voltage well region comprises a high voltage N-well (HVNW) region; wherein the second high voltage well region comprises a high voltage P well (HVPW) region; wherein the dopant of the second semiconductor type comprises N+; and wherein the dopant of the first semiconductor type comprises P+.

11. The method according to Claim 10, wherein depositing the P-doped semiconductor material comprises depositing about 9-10 μm of P-epitaxial doped semiconductor material.

12. The method according to Claim 10, wherein forming the deep N-well region comprises forming the deep N-well region in the entire thickness of the P-doped semiconductor material.

13. The method according to Claim 9, wherein forming the first pad dielectric comprises forming a first pad oxide; wherein forming the second pad dielectric comprises forming a second pad oxide; wherein depositing the dielectric layer comprises depositing a nitride layer; wherein forming the field dielectric comprises forming a field oxide, and wherein forming the gate dielectric comprises forming a gate oxide.

14. A semiconductor device, comprising:

a substrate;

a lateral double-diffused metal oxide semiconductor (LDMOS) device disposed in the substrate, the LDMOS device including a drain;

a first guard ring disposed around and proximate the drain of the LDMOS device; and

a second guard ring disposed around the first guard ring.

15. The method according to Claim 14, wherein the first guard ring and the second guard ring comprise a semiconductive material.

16. The semiconductor device according to Claim 14, wherein the first guard ring comprises a P+ base guard ring, and wherein the second guard ring comprises an N+ collector guard ring.

17. The semiconductor device according to Claim 16, wherein the first guard ring and second guard ring form a parasitic transistor, wherein the parasitic transistor electrically isolates the drain of the LDMOS.

18. The semiconductor device according to Claim 14, wherein the semiconductor comprises an N+ buried layer formed in a top portion of the substrate, and a P-epitaxial layer disposed over the N+ buried layer.

19. The semiconductor device according to Claim 18, wherein the P-epitaxial layer comprises about 9-10 μm of doped semiconductor material.

20. The semiconductor device according to Claim 18, further comprising a deep N-well formed within the P-epitaxial layer, wherein the first or second guard ring is formed in the deep N-well.

21. The semiconductor device according to Claim 20, wherein the deep N-well comprises the entire thickness of the P-epitaxial layer.

22. A lateral double-diffused metal oxide semiconductor (LDMOS) device, comprising:

a substrate, the substrate comprising a first semiconductor type;

a buried layer formed in a top region of the substrate, the buried layer comprising a second semiconductor type;

a doped semiconductor material disposed over the buried layer, the doped semiconductor material being doped with the first semiconductor type;

a deep well region disposed within a portion of the doped semiconductor material, the deep well region comprising an annular ring shape and being doped with the first semiconductor type;

at least one first high voltage well region formed within a portion of the doped semiconductor material;

a second high voltage well region formed within a portion of the doped semiconductor material, the second high voltage well region comprising an annular shape disposed within a central portion of the annular deep well region;

field dielectric disposed over portions of the at least one first high voltage well region and the second high voltage well region;

a gate dielectric disposed over portions of the at least one first high voltage well region, the second high voltage well region, and a portion of the field dielectric;

a gate of the LDMOS device disposed over the gate dielectric;

a source of the LDMOS device formed in the second high voltage well region;

a drain of the LDMOS device formed in the at least one first high voltage well region;

a first guard ring formed in the annular deep well region; and

a second guard ring formed in the second high voltage well region, the second guard ring being formed in a central region of the first guard ring.

23. The LDMOS device according to Claim 22, wherein the first semiconductor type comprises P-type, wherein the second semiconductor type comprises N+, wherein the deep well region comprises an N-well, wherein the at least one first high voltage well region comprises a high voltage N-well (HVNW) region; wherein the second high voltage well region comprises a high voltage P well (HVPW) region; wherein the dopant of the second semiconductor type comprises N+, and wherein the dopant of the first semiconductor type comprises P+.

24. The LDMOS device according to Claim 22, wherein the P-doped semiconductor material comprises about 9-10 μm of P-epitaxial doped semiconductor material.

25. The LDMOS device according to Claim 22, wherein the deep N-well region comprises the entire thickness of the P-doped semiconductor material.

26. The LDMOS device according to Claim 22, wherein the field dielectric comprises a field oxide, and wherein the gate dielectric comprises a gate oxide.